WEST Search History

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DATE: Tuesday, April 06, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L17	clustered vliw	2
☐	L16	variable issue width	10
☐	L15	synchroniz$5 same L14	4
☐	L14	vliw processors	252
☐	L13	multiple vliw cores	0
☐	L12	multiple vliw processors	0
☐	L11	multiple vliw pipelines	0
☐	L10	vliw same L9	20
☐	L9	multiple pipelines	381
☐	L8	vliw and L7	5
☐	L7	5459798.uref.	21
☐	L6	vliw same L5	4
☐	L5	l3 with chip	886
☐	L4	l3 adj chip	45
☐	L3	multiprocessor or multi-processor or (multiple processors)	22457
☐	L2	vliw and L1	6
☐	L1	pipeline paths	24

END OF SEARCH HISTORY

First Hit Fwd Refs

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L17: Entry 2 of 2 File: USPT Feb 15, 2000

US-PAT-NO: 6026479
DOCUMENT-IDENTIFIER: US 6026479 A

TITLE: Apparatus and method for efficient switching of CPU mode between regions of high instruction level parallism and low instruction level parallism in computer programs

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fisher; Joseph A.	Brookline	MA		
Faraboschi; Paolo	Cambridge	MA		
Emerson; Paul G.	San Jose	CA		
Raje; Prasad A.	Fremont	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 064701 [PALM]
DATE FILED: April 22, 1998

INT-CL: [07] G06 F 9/38

US-CL-ISSUED: 712/24; 712/215
US-CL-CURRENT: 712/24; 712/215

FIELD-OF-SEARCH: 712/24, 712/212, 712/215, 712/203

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5442760	August 1995	Rustad	712/24
☐	5457790	October 1995	Iwamura	711/167
☐	5461715	October 1995	Matsuo	712/24
☐	5553276	September 1996	Dean	713/500

☐	5774686	June 1998	Hammond	712/209
☐	5784630	July 1998	Saito	712/30
☐	5850632	December 1998	Robertson	711/170
☐	5860158	January 1999	Pai	711/118
☐	5881296	March 1999	Williams	395/736

OTHER PUBLICATIONS

Joseph A. Fisher, Paolo Faraboschi and Giuseppe Desoli; Hewlett-Packard Laboratories Cambridge, 1 Maine Street, Cambridge, MA 02142; "Custom-Fit Processors: Letting Applications Define Architectures"; 29th Annual IEEE/ACM International Symposium on Microarchitecture; Dec. 2-4, 1996, Paris, France.

ART-UNIT: 273

PRIMARY-EXAMINER: Coleman; Eric

ABSTRACT:

A CPU having a cluster VLIW architecture is shown which operates in both a high instruction level parallelism (ILP) mode and a low ILP mode. In high ILP mode, the CPU executes wide instruction words using all operational clusters of the CPU and all of a main instruction cache and main data cache of the CPU are accessible to a high ILP task. The CPU also includes a mini-instruction cache, a mini-instruction register and a mini-data cache which are inactive during high ILP mode. An instruction level controller in the CPU receives a low ILP signal, such as an interrupt or function call to a low ILP routine, and switches to low ILP mode. In low ILP mode, the main instruction cache and main data cache are deactivated to preserve their contents. At the same time, a predetermined cluster remains active while the remaining clusters are also deactivated. The low ILP task executes instructions from the mini-instruction cache which are input to the predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task. The separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode.

41 Claims, 7 Drawing figures

First Hit Fwd Refs

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L17: Entry 2 of 2 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6026479 A
TITLE: Apparatus and method for efficient switching of CPU mode between regions of high instruction level parallism and low instruction level parallism in computer programs

Brief Summary Text (5):
High performance VLIW central processing units (CPUs) with multiple functional units are designed to obtain improved processing performance by executing code which has high instruction level parallelism (ILP). Clustered VLIW machines (CVLIW) further divide the CPU architecture into clusters which each contain one or more functional units and a separate register file. Instructions in the code are divided into sub-instructions which are input to each cluster and which may be executed in parallel.

Your search matched **23** of **1022101** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

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You may refine your search by editing the current search expression or entering a new one in the text box.

Search

Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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16 **Partitioned schedules for clustered VLIW architectures**
Fernandes, M.M.; Llosa, J.; Topham, N.;
Parallel Processing Symposium, 1998. 1998 IPPS/SPDP. Proceedings of the First Merged International...and Symposium on Parallel and Distributed Processing 1998 , 30 March-3 April 1998
Pages:386 - 391

[Abstract] [PDF Full-Text (552 KB)] **IEEE CNF**

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17 **Flexible compiler-managed L0 buffers for clustered VLIW processors**
Gibert, E.; Sanchez, J.; Gonzalez, A.;
Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on , 2003
Pages:315 - 325

[Abstract] [PDF Full-Text (295 KB)] **IEEE CNF**

---

18 **Exploiting pseudo-schedules to guide data dependence graph partitioning**
Aleta, A.; Codina, J.M.; Sanchez, J.; Gonzalez, A.; Kaeli, D.;
Parallel Architectures and Compilation Techniques, 2002. Proceedings. 2002 International Conference on , 22-25 Sept. 2002

Pages:281 - 290

[Abstract] [PDF Full-Text (337 KB)] **IEEE CNF**

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19 **OneDSP: a unifying DSP architecture for systems-on-a-chip**
Kar-lik Wong; Topham, N.;

Acoustics, Speech, and Signal Processing, 2002. Proceedings. (ICASSP '02). IEEE International Conference on , Volume: 4 , 13-17 May 2002
Pages:IV-3792 - IV-3795 vol.4

[Abstract] [PDF Full-Text (470 KB)] **IEEE CNF**

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20 **Modulo scheduling with integrated register spilling for clustered VLIW architectures**
Zalamea, J.; Llosa, J.; Ayguade, E.; Valero, M.;
Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/IEEE International Symposium on , Dec. 1-5, 2001
Pages:160 - 169

[Abstract] [PDF Full-Text (1085 KB)] **IEEE CNF**

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21 **Instruction scheduling for clustered VLIW DSPs**
Leupers, R.;
Parallel Architectures and Compilation Techniques, 2000. Proceedings. International Conference on , 15-19 Oct. 2000
Pages:291 - 300

[Abstract] [PDF Full-Text (996 KB)] **IEEE CNF**

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22 **Register aware scheduling for distributed cache clustered architecture**
Zhong Wang; Xiaobo Sharon Hu; Sha, E.H.-M.;
Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific , 21-24 Jan. 2003
Pages:71 - 76

[Abstract] [PDF Full-Text (764 KB)] **IEEE CNF**

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23 **A unified modulo scheduling and register allocation technique for clustered processors**
Codina, J.M.; Sanchez, J.; Gonzalez, A.;
Parallel Architectures and Compilation Techniques, 2001. Proceedings. 2001 International Conference on , 8-12 Sept. 2001
Pages:175 - 184

[Abstract] [PDF Full-Text (960 KB)] **IEEE CNF**

Prev 1 2

First Hit Fwd Refs

End of Result Set

☐ Generate Collection | Print

L2: Entry 6 of 6 File: USPT Oct 7, 2003

US-PAT-NO: 6631439
DOCUMENT-IDENTIFIER: US 6631439 B2

TITLE: VLIW computer processing architecture with on-chip dynamic RAM

DATE-ISSUED: October 7, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Saulsbury; Ashley	Los Gatos	CA		
Nettleton; Nyles	Campbell	CA		
Parkin; Michael	Palo Alto	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 802324 [PALM]
DATE FILED: March 8, 2001

PARENT-CASE:
CROSS-REFERENCES TO RELATED APPLICATIONS This applications claims the benefit of U.S. Provisional Patent Application Ser. No. 60/187,796, filed on Mar. 8, 2000 and entitled "VLIW Computer Processing Architecture with On-Chip Dynamic RAM," the entirety of which is incorporated by reference herein for all purposes.

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/104; 711/101, 711/105, 711/170, 711/171, 711/172
US-CL-CURRENT: 711/104; 711/101, 711/105, 711/170, 711/171, 711/172

FIELD-OF-SEARCH: 711/101, 711/104, 711/105, 711/1, 711/170-172

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4725945	February 1988	Kronstadt et al.	711/106
☐	4894770	January 1990	Ward et al.	711/128

☐	4980819	December 1990	Cushing et al.	
☐	5184320	February 1993	Dye	365/49
☐	5261066	November 1993	Jouppi et al.	711/122
☐	5301340	April 1994	Cook	
☐	5317718	May 1994	Jouppi	711/137
☐	5386547	January 1995	Jouppi	711/122
☐	5530817	June 1996	Masubuchi	
☐	5564035	October 1996	Lai	711/144
☐	5588130	December 1996	Fujishima et al.	711/118
☐	5623627	April 1997	Witt	711/122
☐	5649154	July 1997	Kumar et al.	711/122
☐	5650955	July 1997	Puar et al.	365/51
☐	5687338	November 1997	Boggs et al.	712/205
☐	5703806	December 1997	Puar et al.	365/181
☐	5900011	May 1999	Saulsbury et al.	711/119
☐	5953738	September 1999	Rao	711/105
☐	6128702	October 2000	Saulsbury et al.	711/133
☐	6202143	March 2001	Rim	710/107
☐	6256256	July 2001	Rao	365/149
☐	6321318	November 2001	Baltz et al.	711/154

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
WO 00/33178	June 2000	WO	

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Mitsubishi Electric Corp; Product Specification for Single-Chip CMOS Microcomputer; May 1998.*
Numomura Y et al: "M32R/D-Integrating DRAM and Microprocessor" IEEE Inc. New York, US, vol. 17 No. 6, Nov. 1, 1997, pp. 40-48, XP000726003; ISSN: 0272-1732.
Kozyrakis C E et al: "Scalable Processors in the Billion-Transistor Era: IRAM" Computer, IEEE Computer Society, Long Beach., CA, US, US vol. 20, No. 0 Sep. 1, 1997, pp. 75-78, XP000730003; ISSN: 0018-9162.
Herrmann Klaus, Hilgenstock Joerg, Pirsch Peter: "Architecture of a Multiprocessor System with Embedded DRAM for Large Area Integration" Oct. 8, 1997, IEEE International Conference on Innovative Systems in Silicon, Piscataway, NJ, USA; XP002179990.
Aimoto, Yoshiharu et al.; "A.768GIPS 3.84GB/s 1 W Parallel Image-Processing RAM Integrating a 16 Mb DRAM and 128 Processors"; ISSCC96/Session 23 / DRAM / Paper SP23.3; 1996 IEEE International Solid-State Circuits Conference; pp. 372-373 and 476.
Bursky, Dave; "Combo RISC CPU and DRAM Solves Data Bandwidth Issues"; Electronic Design; Mar. 4, 1996; pp. 67-71.

Saulsbury, Ashley, et al., "Missing the Memory Wall: The Case for Processor/Memory Integration"; ACM; 1996; pp. 90-101.
Shimizu, Toro, et al.; "A Multimedia 32b RISC Microprocessor with 16 Mb DRAM"; ISSCC96/Session 13 / Microprocessors/Paper FP 13.4; 1996 IEEE International Solid State Circuits Conference; pp. 216-217 and 448.
Mitsubishi Electric Corp; Product Specification for Single-Chip 32-Bit CMOS Microcomputer; .COPYRGT. May 1998.

ART-UNIT: 2187

PRIMARY-EXAMINER: Nguyen; T. V.

ATTY-AGENT-FIRM: Townsend and Townsend and Crew LLP

ABSTRACT:

A novel processor chip (10) having a processing core (12), at least one bank of memory (14), an I/O link (26) configured to communicate with other like processor chips or compatible I/O devices, a memory controller (20) in electrical communication with processing core (12) and memory (14), and a distributed shared memory controller (22) in electrical communication with memory controller (20) and I/O link (26). Distributed shared memory controller (22) is configured to control the exchange of data between processor chip (10) and the other processor chips or I/O devices. In addition, memory controller (20) is configured to receive memory requests from processing core (12) and distributed shared memory controller (22) and process the memory request with memory (14). Processor chip (10) may further comprise an external memory interface (24) in electrical communication with memory controller (20). External memory interface (24) is configured to connect processor chip (10) with external memory, such as DRAM. Memory controller (20) is configured to receive memory requests from processing core (12) and distributed shared memory controller (22), determine whether the memory requests are directed to memory (14) on chip (10) or the external memory, and process the memory requests with memory (14) on processor chip (10) or with the external memory through external memory interface (24).

37 Claims, 5 Drawing figures

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L8: Entry 19 of 22 File: DWPI Jul 31, 1997

DERWENT-ACC-NO: 1997-470440
DERWENT-WEEK: 200255

TITLE: Array bounds checking apparatus - includes comparison elements verifying that referenced element is between maximum and minimum array size boundary values by comparison

INVENTOR: JOY, W N; O'CONNOR, J M ; TREMBLAY, M ; OCONNOR, J M

PATENT-ASSIGNEE:

ASSIGNEE	CODE
SUN MICROSYSTEMS INC	SUNM

PRIORITY-DATA: 1996US-0642248 (May 2, 1996), 1996US-010527P (January 24, 1996)

Search Selected Search ALL Clear

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 9727544 A1	July 31, 1997	E	199	G06F012/14
DE 69713400 E	July 18, 2002		000	G06F012/14
EP 976050 A1	February 2, 2000	E	000	
JP 2000501217 W	February 2, 2000		086	G06F011/28
KR 99081958 A	November 15, 1999		000	G06F012/14
EP 976050 B1	June 12, 2002	E	000	G06F012/14

DESIGNATED-STATES: CN JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE DE FR GB NL SE DE FR GB NL SE

CITED-DOCUMENTS:1.Jnl.Ref; EP 17670 ; EP 214490 ; EP 535538 ; JP 4071050 ; US 3573855

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
WO 9727544A1	January 23, 1997	1997WO-US01305	
DE 69713400E	January 23, 1997	1997DE-0613400	
DE 69713400E	January 23, 1997	1997EP-0904011	
DE 69713400E	January 23, 1997	1997WO-US01305	
DE 69713400E		EP 976050	Based on
DE 69713400E		WO 9727544	Based on

EP 976050A1	January 23, 1997	1997EP-0904011	
EP 976050A1	January 23, 1997	1997WO-US01305	
EP 976050A1		WO 9727544	Based on
JP2000501217W	January 23, 1997	1997JP-0527086	
JP2000501217W	January 23, 1997	1997WO-US01305	
JP2000501217W		WO 9727544	Based on
KR 99081958A	January 23, 1997	1997WO-US01305	
KR 99081958A	July 22, 1998	1998KR-0705676	
KR 99081958A		WO 9727544	Based on
EP 976050B1	January 23, 1997	1997EP-0904011	
EP 976050B1	January 23, 1997	1997WO-US01305	
EP 976050B1		WO 9727544	Based on

INT-CL (IPC): G06 F 11/28; G06 F 12/14

RELATED-ACC-NO: 1997-393871;1997-393873 ;1997-470439

ABSTRACTED-PUB-NO: EP 976050B
BASIC-ABSTRACT:

The array bounds checking apparatus includes an associative memory element which is configured to store and retrieve array size values associated with array access instructions. Each array access instruction references a value of an element in the array.

A comparison element is coupled to an output of the associative memory element. This comparison element compares a given maximum array size with the value of the referenced element so as to provide a maximum violation signal. A second comparison element compares a given minimum array size and the value of the referenced element so as to provide a minimum violation signal.

ADVANTAGE - Reduces time required to retrieve array information and verify size.
ABSTRACTED-PUB-NO:

WO 9727544A
EQUIVALENT-ABSTRACTS:

The array bounds checking apparatus includes an associative memory element which is configured to store and retrieve array size values associated with array access instructions. Each array access instruction references a value of an element in the array.

A comparison element is coupled to an output of the associative memory element. This comparison element compares a given maximum array size with the value of the referenced element so as to provide a maximum violation signal. A second comparison element compares a given minimum array size and the value of the referenced element so as to provide a minimum violation signal.

ADVANTAGE - Reduces time required to retrieve array information and verify size.

CHOSEN-DRAWING: Dwg.6a/6

TITLE-TERMS: ARRAY BOUND CHECK APPARATUS COMPARE ELEMENT VERIFICATION REFERENCE

ELEMENT MAXIMUM MINIMUM ARRAY SIZE BOUNDARY VALUE COMPARE

DERWENT-CLASS: T01

EPI-CODES: T01-H01C2;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1997-392565

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L6: Entry 4 of 4 File: USPT Oct 17, 1995

US-PAT-NO: 5459798
DOCUMENT-IDENTIFIER: US 5459798 A
** See image for Certificate of Correction **

TITLE: System and method of pattern recognition employing a multiprocessing pipelined apparatus with private pattern memory

DATE-ISSUED: October 17, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bailey; Delbert D.	Aptos	CA		
Dulong; Carole	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 060579 [PALM]
DATE FILED: May 12, 1993

PARENT-CASE:
1. Related US Application The present invention is a continuation in part of application Ser. No. 08/034,678 filed Mar. 19, 1993, entitled, "A Memory Transfer Apparatus and Method Useful Within a Pattern Recognition System" and assigned to the assignee of the present invention.

INT-CL: [06] G06 K 9/68

US-CL-ISSUED: 382/218; 382/303, 364/231.8, 364/DIG.1, 364/926.8, 364/948.34, 364/DIG.2
US-CL-CURRENT: 382/218; 382/303, 704/231, 712/24

FIELD-OF-SEARCH: 382/13, 382/30, 382/33, 382/34, 382/41, 382/49, 364/229.2, 364/231.8, 364/240.1, 364/240.2, 364/242.3, 364/243, 364/243.43, 364/243.44, 364/243.45, 364/926.8, 364/948.34, 364/964

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

☐	4395699	July 1983	Sternberg	382/41
☐	4790026	December 1988	Gennery et al.	382/49
☐	5014327	May 1991	Potter et al.	382/14
☐	5111512	May 1992	Fan et al.	382/3
☐	5226091	July 1993	Howell et al.	382/3
☐	5265174	November 1993	Nakatsuka	382/38

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0550865	July 1993	EP	382/13
56122445	February 1983	JP	382/34
62-117744	November 1988	JP	382/34

OTHER PUBLICATIONS

English Translation of Japanese Kokai 58-24975 (to Komiya, publ. Feb. 1983).
English Translation of Japanese Kokai 63-282586 (to Minewaki, publ. Nov. 1988).

ART-UNIT: 266

PRIMARY-EXAMINER: Boudreau; Leo H.

ASSISTANT-EXAMINER: Johns; Andrew W.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A computer implemented apparatus and method of pattern recognition utilizing a pattern recognition engine coupled with a general purpose computer system. The present invention system provides increased accuracy and performance in handwriting and voice recognition systems and may interface with general purpose computer systems. A pattern recognition engine is provided within the present invention that contains five pipelines which operate in parallel and are specially optimized for Dynamic Time Warping and Hidden Markov Models procedures for pattern recognition, especially handwriting recognition. These pipelines comprise two arithmetic pipelines, one control pipeline and two pointer pipelines. Further, a private memory is associated with each pattern recognition engine for library storage of reference or prototype patterns. Recognition procedures are partitioned across a CPU and the pattern recognition engine. Use of a private memory allows quick access of the library patterns without impeding the performance of programs operating on the main CPU or the host bus. Communication between the CPU and the pattern recognition engine is accomplished over the host bus.

50 Claims, 18 Drawing figures

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L6: Entry 4 of 4 File: USPT Oct 17, 1995

DOCUMENT-IDENTIFIER: US 5459798 A

**** See image for Certificate of Correction ****

TITLE: System and method of pattern recognition employing a multiprocessing pipelined apparatus with private pattern memory

Detailed Description Text (33):

The pertinent components of the pattern recognition engine 525 (programmable multiprocessor) are illustrated in FIG. 5, which except for the external memory 615 are located within a single chip package. FIG. 5 also illustrates the communication bus architecture shared between the components of the PR engine 525. Each pattern recognition engine contains: a program memory 415, two data memories 30 and 32, a memory controller 419, a memory to memory transfer block 416, a VLIW execution block 417 and a system bus interface block 418. It is appreciated that any of the well known system bus interface technologies may be utilized within the present invention PR engine. The execution unit 430 is comprised of program memory block 415, data memories 30 and 32 and VLIW execution block 417 as well as other elements to be described below. Interfaced to each PR engine 525 is a private memory block 615 as discussed above. The system bus interface 418 is coupled to the ISA system bus 100. Each of the above blocks, where pertinent to the discussions of the present invention, will be described in greater detail to follow. It is appreciated that the program memory 415 may be loaded with the lower level procedures by the CPU 510 directing transfers from the disk 516 or RAM 512.

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L15: Entry 2 of 4 File: PGPB Nov 15, 2001

PGPUB-DOCUMENT-NUMBER: 20010042187
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010042187 A1

TITLE: VARIABLE ISSUE-WIDTH VLIW PROCESSOR

PUBLICATION-DATE: November 15, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
TREMBLAY, MARC	MENLO PARK	CA	US	

APPL-NO: 09/ 204536 [PALM]
DATE FILED: December 3, 1998

CONTINUED PROSECUTION APPLICATION: CPA

INT-CL: [07] G06 F 15/00, G06 F 9/00

US-CL-PUBLISHED: 712/2; 709/107
US-CL-CURRENT: 712/2; 718/107

REPRESENTATIVE-FIGURES: 9

ABSTRACT:

Abstract of the Disclosure A processor has a flexible architecture that efficiently handles computing applications having a range of instruction-level parallelism from a very low degree to a very high degree of instruction-level parallelism. The processor includes a plurality of processing units, an individual processing unit of the plurality of processing units including a multiple-instruction parallel execution path. For computing applications having a low degree of instruction-level parallelism, the processor includes control logic that controls the plurality of processing units to execute instructions mutually independently in a plurality of independent execution threads. For computing applications having a high degree of instruction-level parallelism, the processor further includes control logic that controls the plurality of processing units with a low thread synchronization to operate in combination using spatial software pipelining in the manner of a single wide-issue processor. The control logic in the processor alternatively controls the plurality of processing units to operate: (1) in a multiple-thread operation on the basis of a highly parallel structure including multiple independent parallel execution paths for executing in parallel across threads and a multiple-instruction parallel pathway within a thread, and (2) in a single-thread wide-issue operation on the basis of the highly parallel structure including multiple parallel execution paths with low level synchronization for executing the single wide-issue thread. The multiple independent parallel execution paths include functional units that execute an instruction set including special data-handling instructions that are advantageous in a multiple-thread environment.

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L15: Entry 2 of 4 File: PGPB Nov 15, 2001

DOCUMENT-IDENTIFIER: US 20010042187 A1
TITLE: VARIABLE ISSUE-WIDTH VLIW PROCESSOR

Summary of Invention Paragraph:
[0015] For applications with a high level of instruction-level parallelism, the VLIW processor executes a plurality of instructions in parallel on the plurality of independent processors using low thread synchronization overhead to operate with the same level of performance as an increased width VLIW processor. For example, in an illustrative embodiment, a VLIW processor includes two independent four-wide VLIW processors to selectively operate either as an eight-wide VLIW processor or two independent four-wide VLIW processors that mutually execute separate threads. Each of the independent processors includes a very rich set of functional units to form, in combination, a highly powerful processor, without the complexity of implementing the extensive control circuitry and connections of an eight-wide VLIW processor.

Detail Description Paragraph:
[0059] The illustrative VLIW processor 100 executes a plurality of instructions in parallel on the plurality of independent processors using low thread synchronization overhead to operate with the same level of performance as an increased width VLIW processor. For applications with a high level of instruction-level parallelism, the VLIW processor 100 utilizes the two independent four-wide VLIW processors, media processing units 110 and 112, to selectively operate either as an eight-wide VLIW processor or two independent four-wide VLIW processors that mutually execute separate threads. The independent media processing units 110 and 112 each includes a very rich set of functional units to form, in combination, a highly powerful processor without the complexity of implementing the extensive control circuitry and connections of an eight-wide VLIW processor.

Detail Description Paragraph:
[0076] Referring to FIG. 5B, a schematic block diagram illustrates a logical view of a combination of two independent processors to form a wide-VLIW processor 100. Each of the illustrative VLIW processors includes an instruction buffer 214, a register file 216, and four functional units arranged in a group of three media functional units 220, and one general functional unit 222. The instruction buffer 214 in each of the independent processors supplies up to four subinstructions to the register file 216. The up to four subinstructions execute on the media functional units 220 and the general functional unit 222. For applications with a high level of instruction-level parallelism, the eight-wide VLIW processor 100 executes a plurality of instructions in parallel on the plurality of independent processors using low thread synchronization overhead to operate with the same level of performance as an increased width VLIW processor. The VLIW processor 100 includes two independent four-wide VLIW processors 110 and 112 to selectively operate either as an eight-wide VLIW processor or two independent four-wide VLIW processors that mutually execute separate threads. The independent processors includes a very rich set of functional units to form, in combination, a highly powerful processor, without the complexity of implementing the extensive control circuitry and connections of the eight-wide VLIW processor.

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L8: Entry 14 of 22 File: DWPI Jun 18, 2003

DERWENT-ACC-NO: 2000-423048
DERWENT-WEEK: 200348

TITLE: Very long instruction word processor has global and local registers accessible by functional units, and a functional unit associated with register file segment containing local register, respectively

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PRIORITY-DATA: 1998US-0204585 (December 3, 1998)

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PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	DE 69907955 E	June 18, 2003		000	G06F009/30
☐	WO 200033178 A1	June 8, 2000	E	033	G06F009/30
☐	EP 1137982 A1	October 4, 2001	E	000	G06F009/30
☐	US 20010042190 A1	November 15, 2001		000	G06F015/00
☐	EP 1137982 B1	May 14, 2003	E	000	G06F009/30

DESIGNATED-STATES: JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE DE GB

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
DE 69907955E	December 3, 1999	1999DE-0607955	
DE 69907955E	December 3, 1999	1999EP-0965130	
DE 69907955E	December 3, 1999	1999WO-US28820	
DE 69907955E		EP 1137982	Based on
DE 69907955E		WO 200033178	Based on
WO 200033178A1	December 3, 1999	1999WO-US28820	
EP 1137982A1	December 3, 1999	1999EP-0965130	
EP 1137982A1	December 3, 1999	1999WO-US28820	
EP 1137982A1		WO 200033178	Based on
US20010042190A1	December 3, 1998	1998US-0204585	
EP 1137982B1	December 3, 1999	1999EP-0965130	
EP 1137982B1	December 3, 1999	1999WO-US28820	

EP 1137982B1 WO 200033178 Based on

INT-CL (IPC): G06 F 9/26; G06 F 9/30; G06 F 12/00; G06 F 15/00

ABSTRACTED-PUB-NO: US20010042190A
BASIC-ABSTRACT:

NOVELTY - The processor has a multi-ported register file (600) divided into register file segments (610,612,614,616). One of the segments is coupled to and associated with one of functional units. The segments in turn are divided into global and local registers that are accessible by functional units, and a functional unit associated with the register file segment containing the local registers, respectively.

DETAILED DESCRIPTION - The register file is coupled to the decoder which decodes very long instruction word including several sub-instructions being allocated into positions of the instruction word. The local and global registers are addressed using register addresses in an address space that is defined for a register file segment/functional unit pair. An INDEPENDENT CLAIM is also included for operating method of very long instruction word processor.

USE - Very long instruction word (VLIW) processor.

ADVANTAGE - Provides split register which allows reduced size and improved performance through faster access. Wastage of registers is avoided in the processor, by supporting individual marking of registers.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic block diagram of register file for VLIW processor.

Multi-ported register file 600

Register file segments 610,612,614,616

ABSTRACTED-PUB-NO: WO 200033178A
EQUIVALENT-ABSTRACTS:

NOVELTY - The processor has a multi-ported register file (600) divided into register file segments (610,612,614,616). One of the segments is coupled to and associated with one of functional units. The segments in turn are divided into global and local registers that are accessible by functional units, and a functional unit associated with the register file segment containing the local registers, respectively.

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Multi-ported register file 600

Register file segments 610,612,614,616

CHOSEN-DRAWING: Dwg.6/10

DERWENT-CLASS: T01
EPI-CODES: T01-F03A; T01-J11A;

LOCAL AND GLOBAL REGISTER PARTITIONING IN A VLIW PROCESSOR

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Publication date: 2001-11-15
Inventor: JOY WILLIAM (US); TREMBLAY MARC (US)
Applicant:
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- european: G06F9/30R4S; G06F9/38E6
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Abstract of **US2001042190**

A Very Long Instruction Word (VLIW) processor having a plurality of functional units includes a multi-ported register file that is divided into a plurality of separate register file segments, each of the register file segments being associated to one of the plurality of functional units. The register file segments are partitioned into local registers and global registers. The global registers are read and written by all functional units. The local registers are read and written only by a functional unit associated with a particular register file segment. The local registers and global registers are addressed using register addresses in an address space that is separately defined for a register file segment/functional unit pair. The global registers are addressed within a selected global register range using the same register addresses for the plurality of register file segment/functional unit pairs. The local registers in a register file segment are addressed using register addresses in a local register range outside the global register range that are assigned within a single register file segment/functional unit pair. Register addresses in the local register range are the same for the plurality of register file segment/functional unit pairs and address registers locally within a register file segment/functional unit pair